

Figure 1

FIG. 2 is a block diagram of a system 200, according to one embodiment of the present invention. The system 200 includes a processor 202a, a memory 202b, and a plurality of input/output devices 204a-204f, 204n. The processor 202a is connected to the memory 202b and the input/output devices 204a-204f, 204n. The input/output devices 204a-204f, 204n are connected to the processor 202a and the memory 202b. The system 200 is configured to execute a program stored in the memory 202b, and to receive data from the input/output devices 204a-204f, 204n. The system 200 is also configured to output data to the input/output devices 204a-204f, 204n. The system 200 is further configured to store data in the memory 202b. The system 200 is also configured to retrieve data from the memory 202b. The system 200 is configured to execute a program stored in the memory 202b, and to receive data from the input/output devices 204a-204f, 204n. The system 200 is also configured to output data to the input/output devices 204a-204f, 204n. The system 200 is further configured to store data in the memory 202b. The system 200 is also configured to retrieve data from the memory 202b.

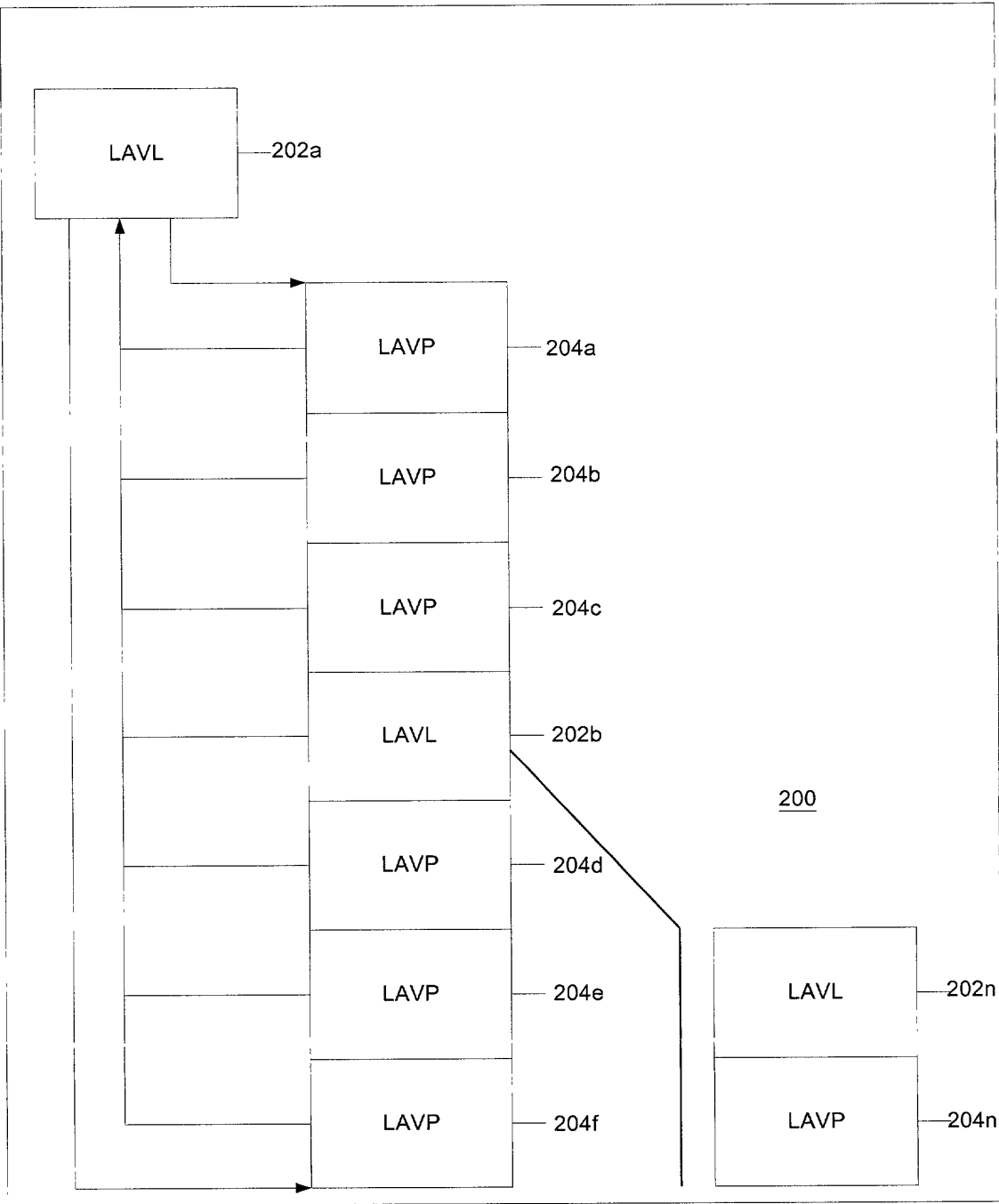


Figure 2

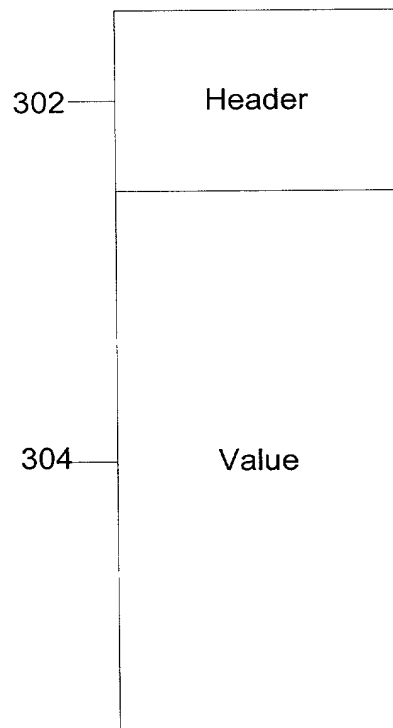


Figure 3A



the first and second strings are compared to determine if the first string is a substring of the second string.

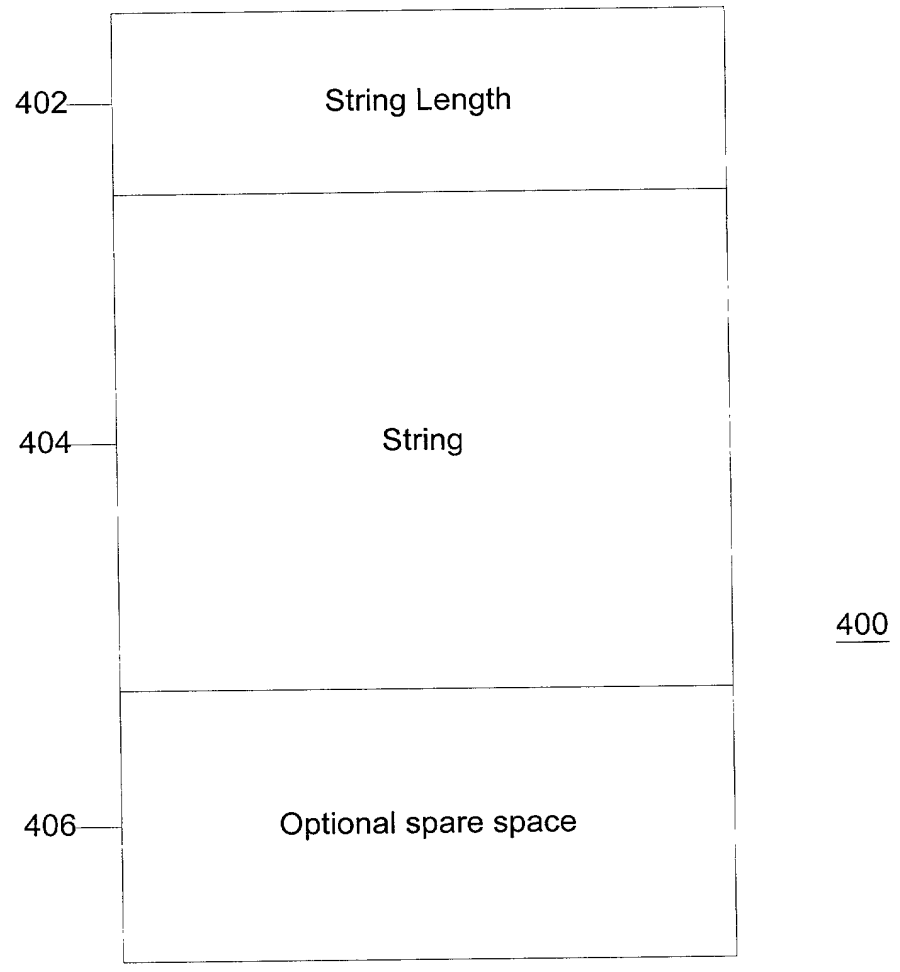


Figure 4



Figure 5

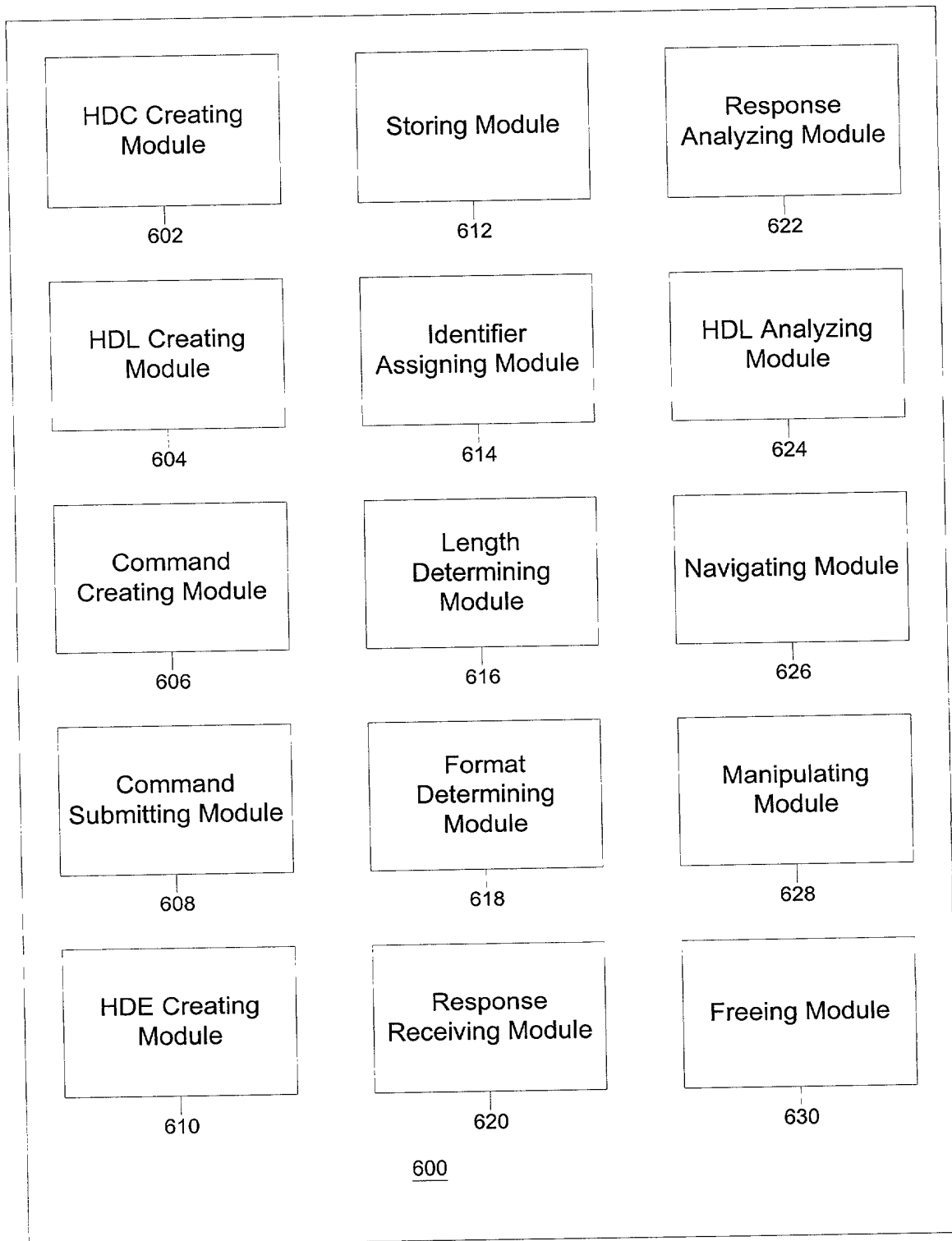


Figure 6A

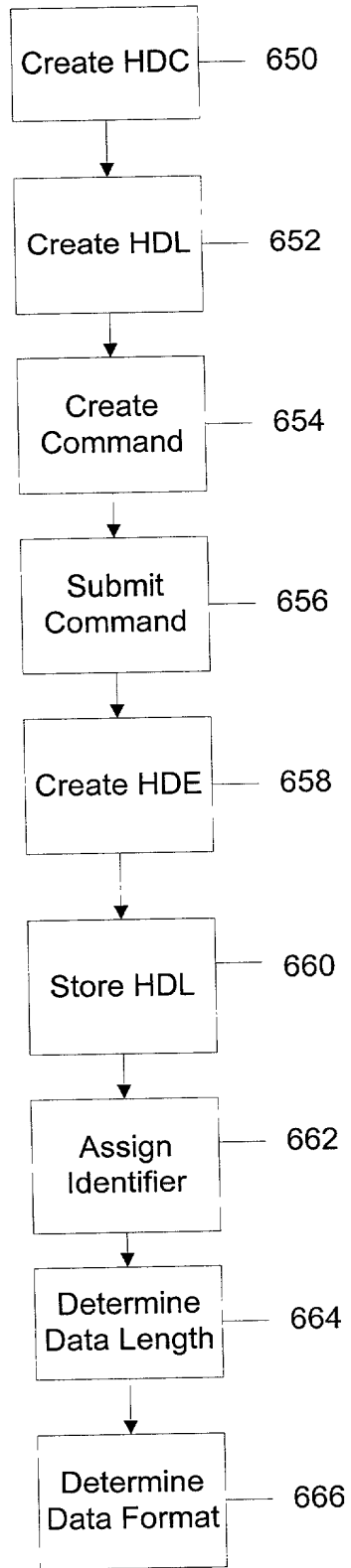


Figure 6B



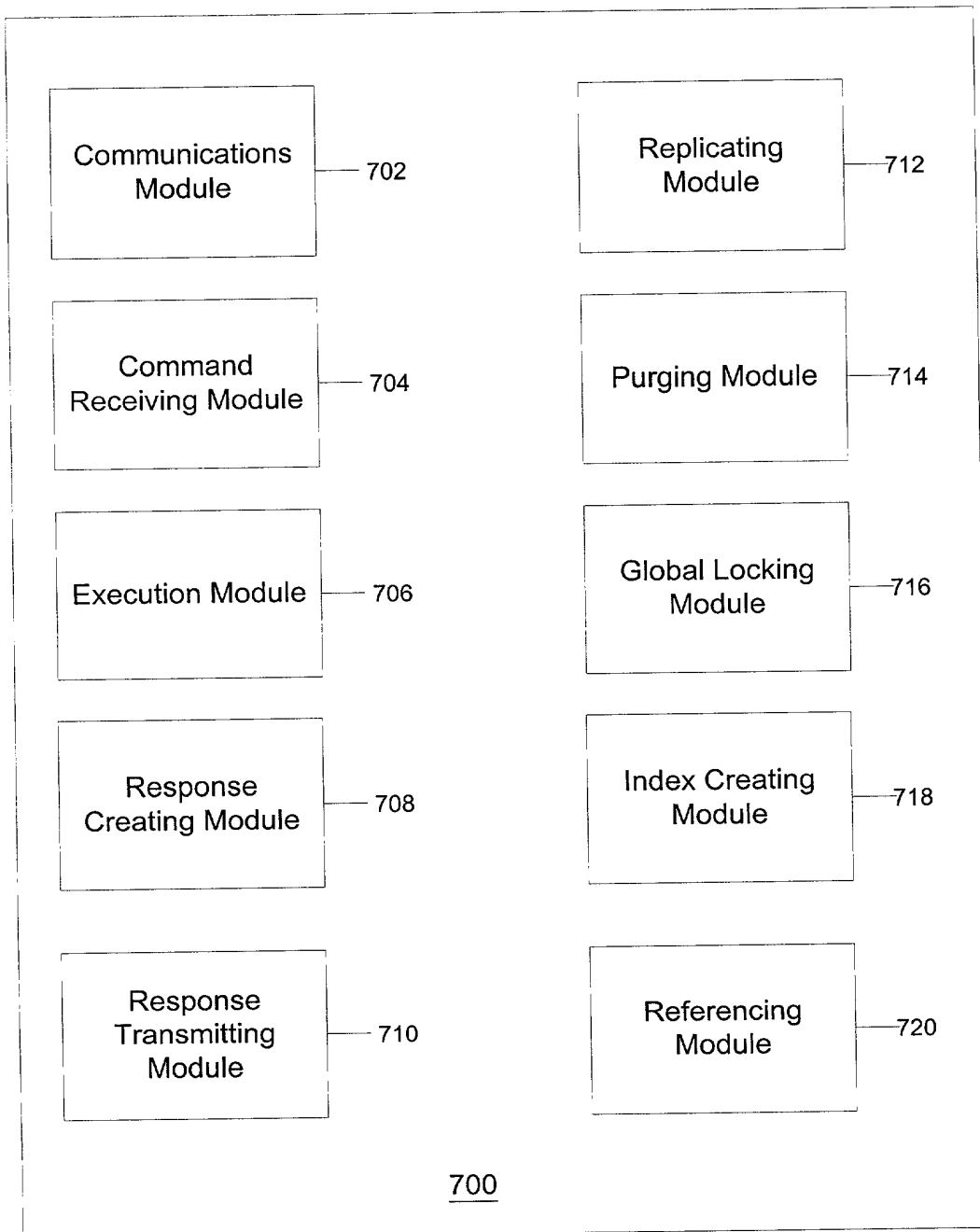


Figure 7

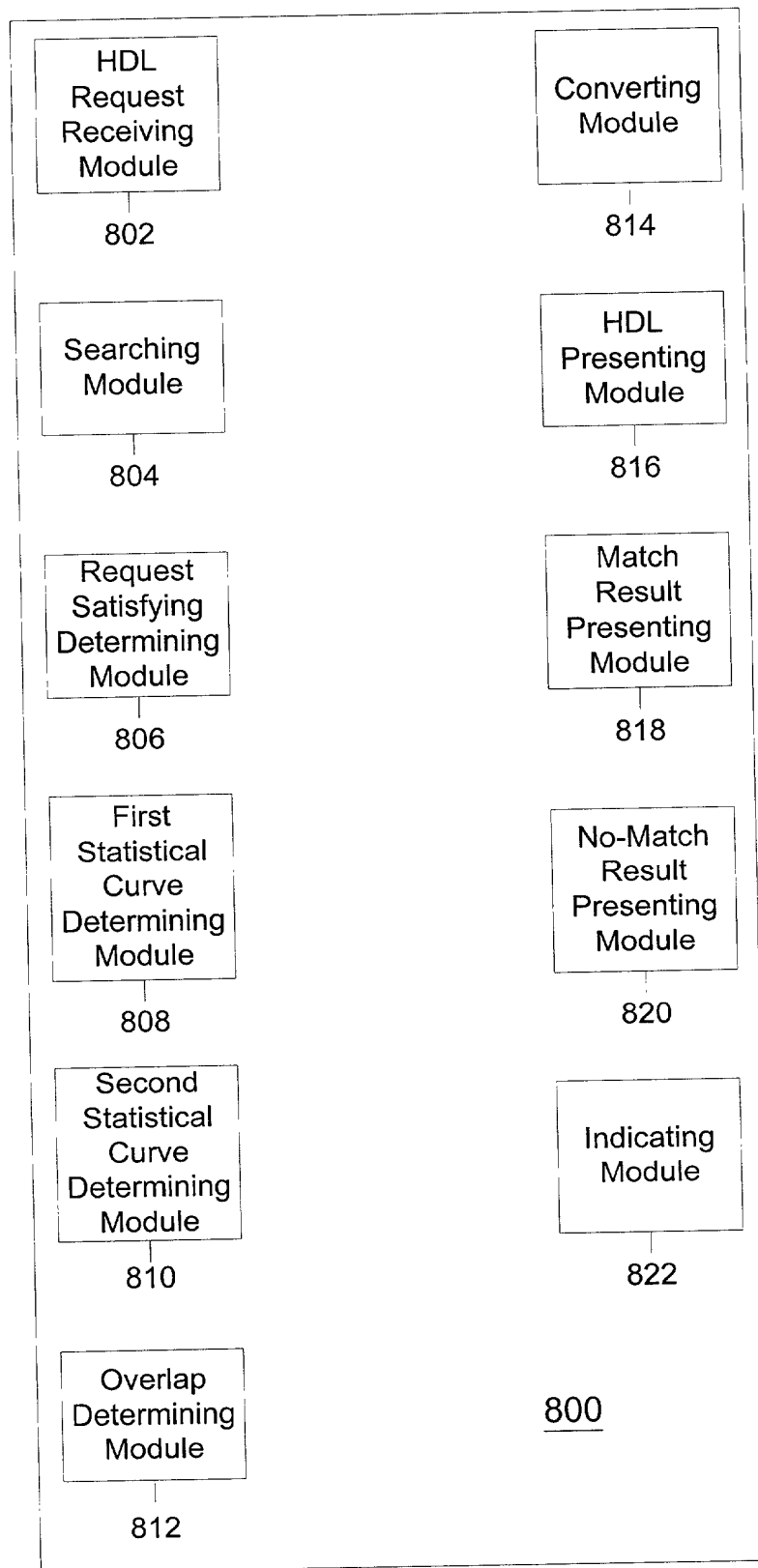


Figure 8



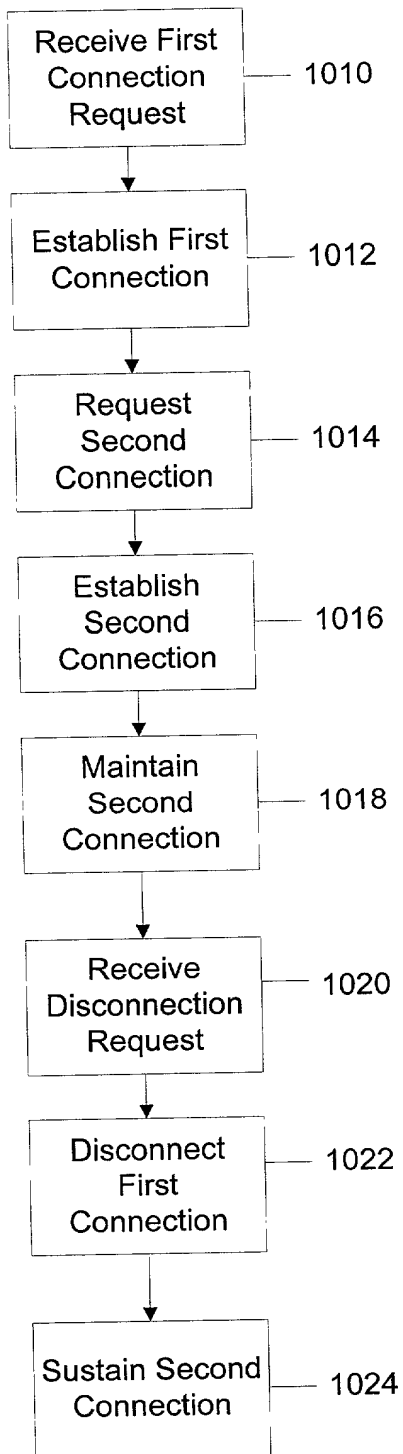


Figure 10

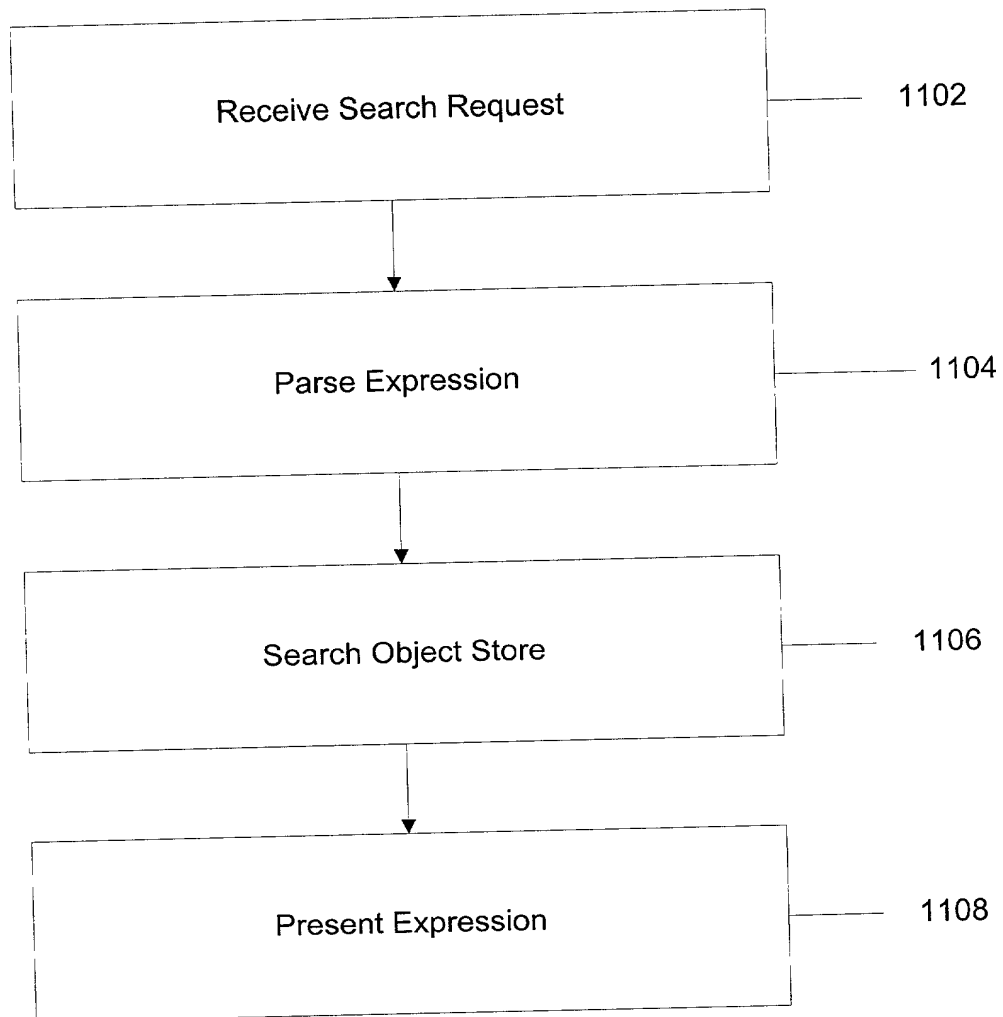


Figure 11

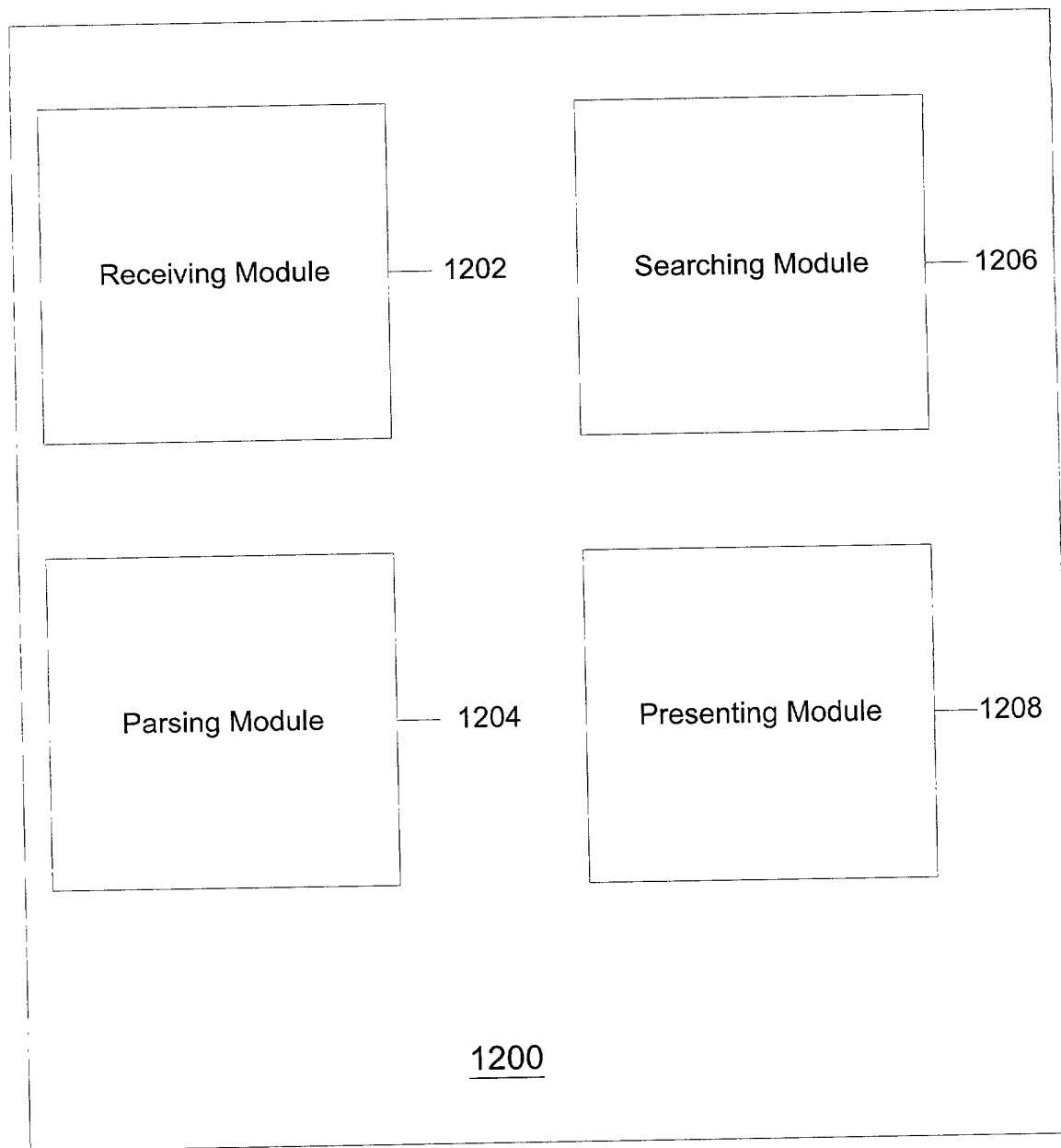


Figure 12

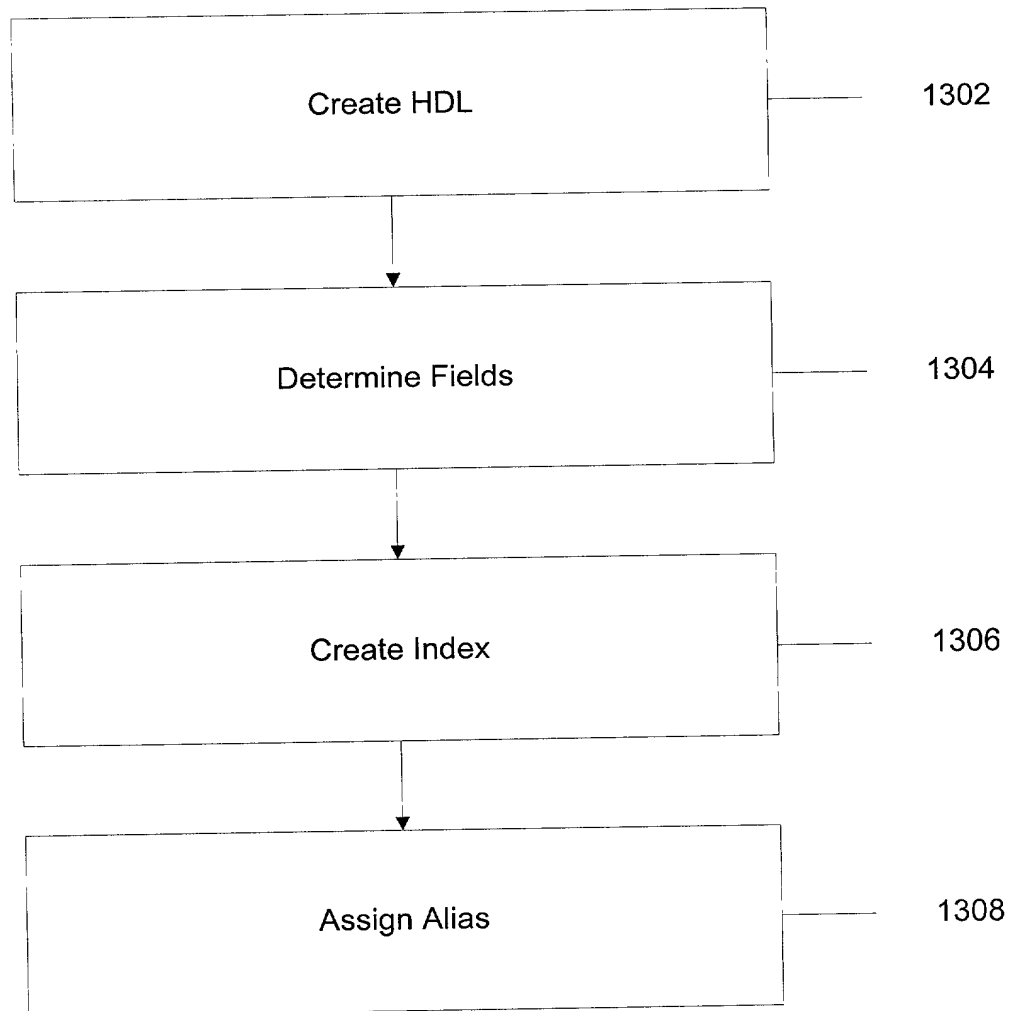


Figure 13

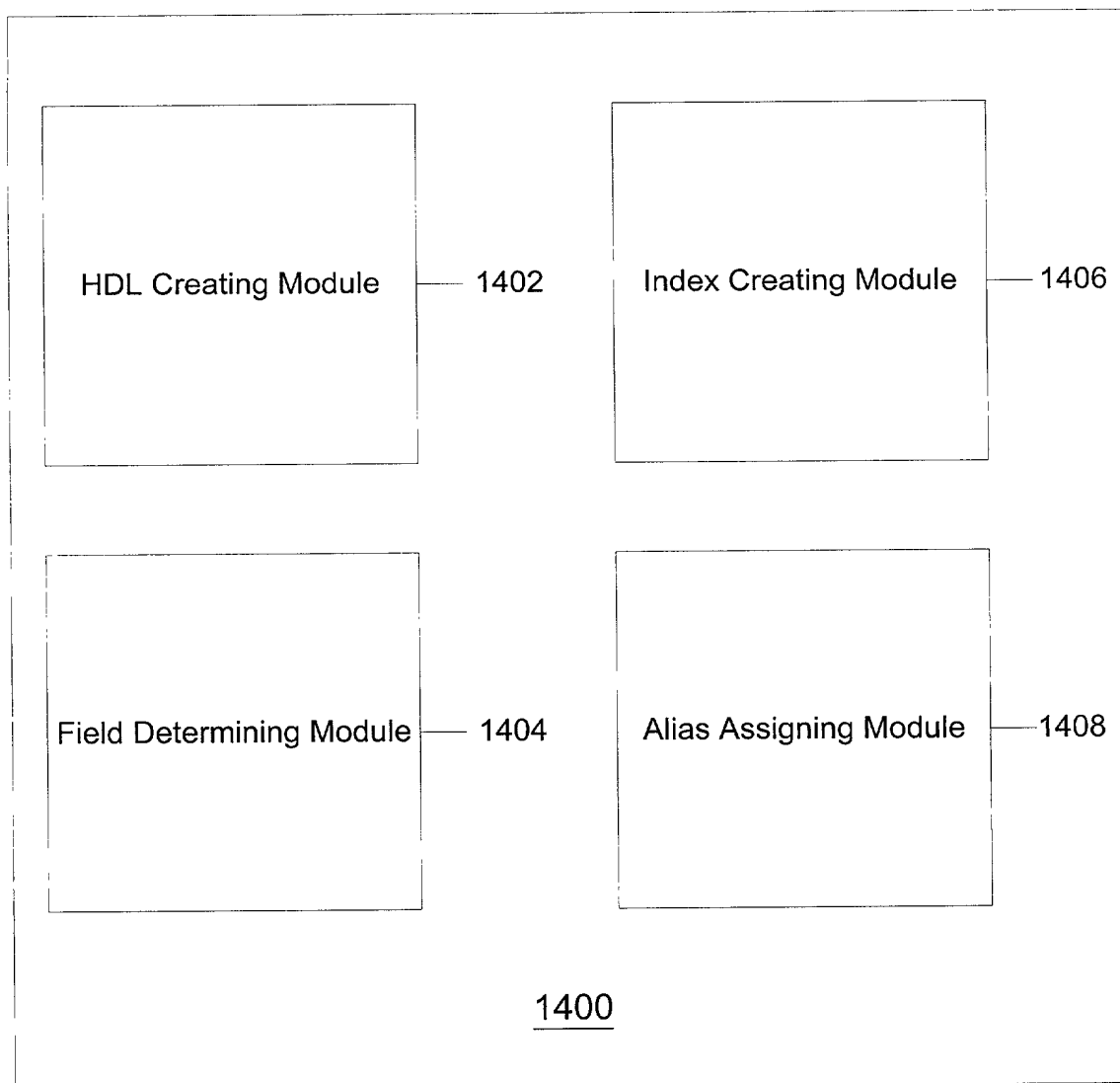


Figure 14



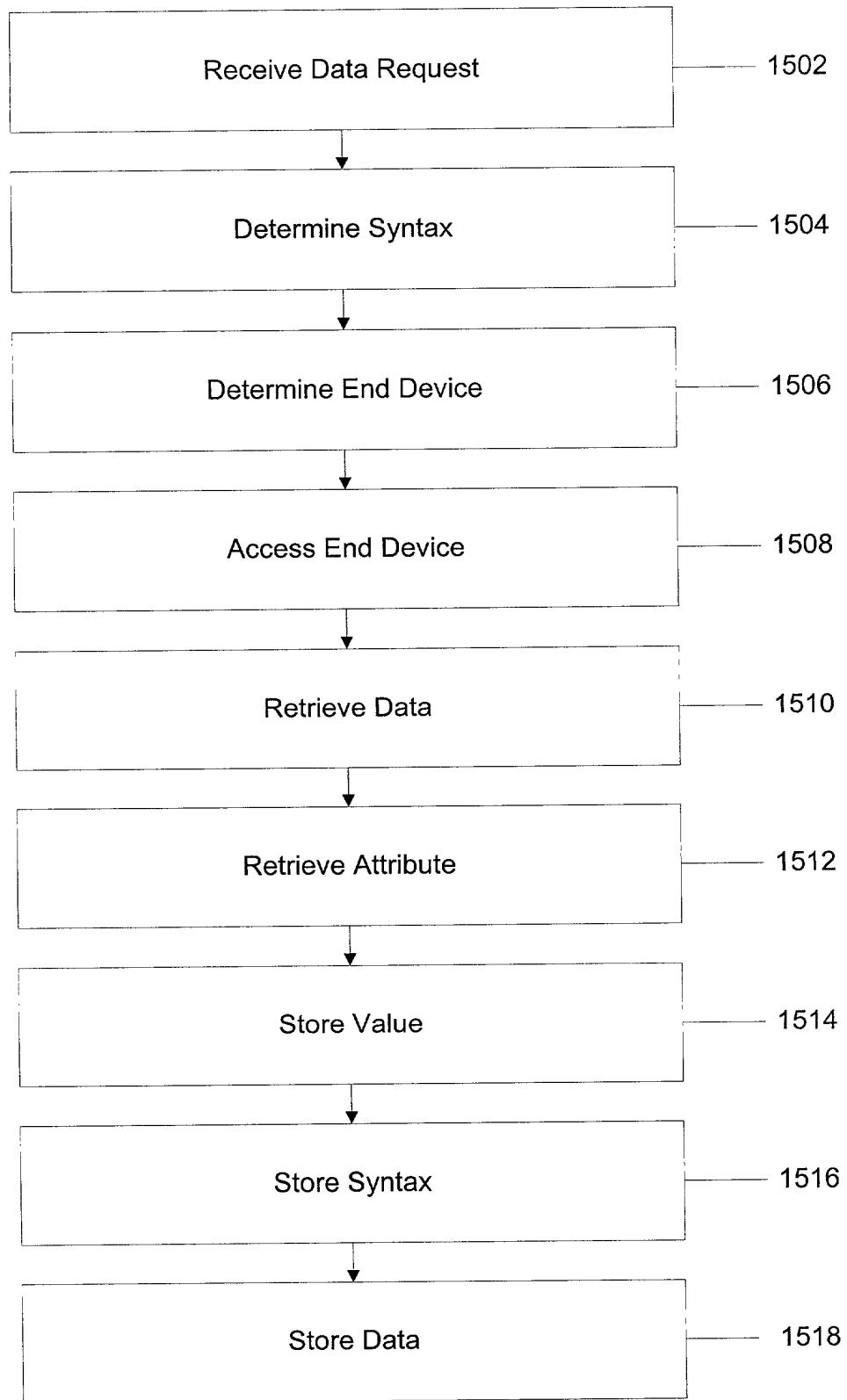


Figure 15

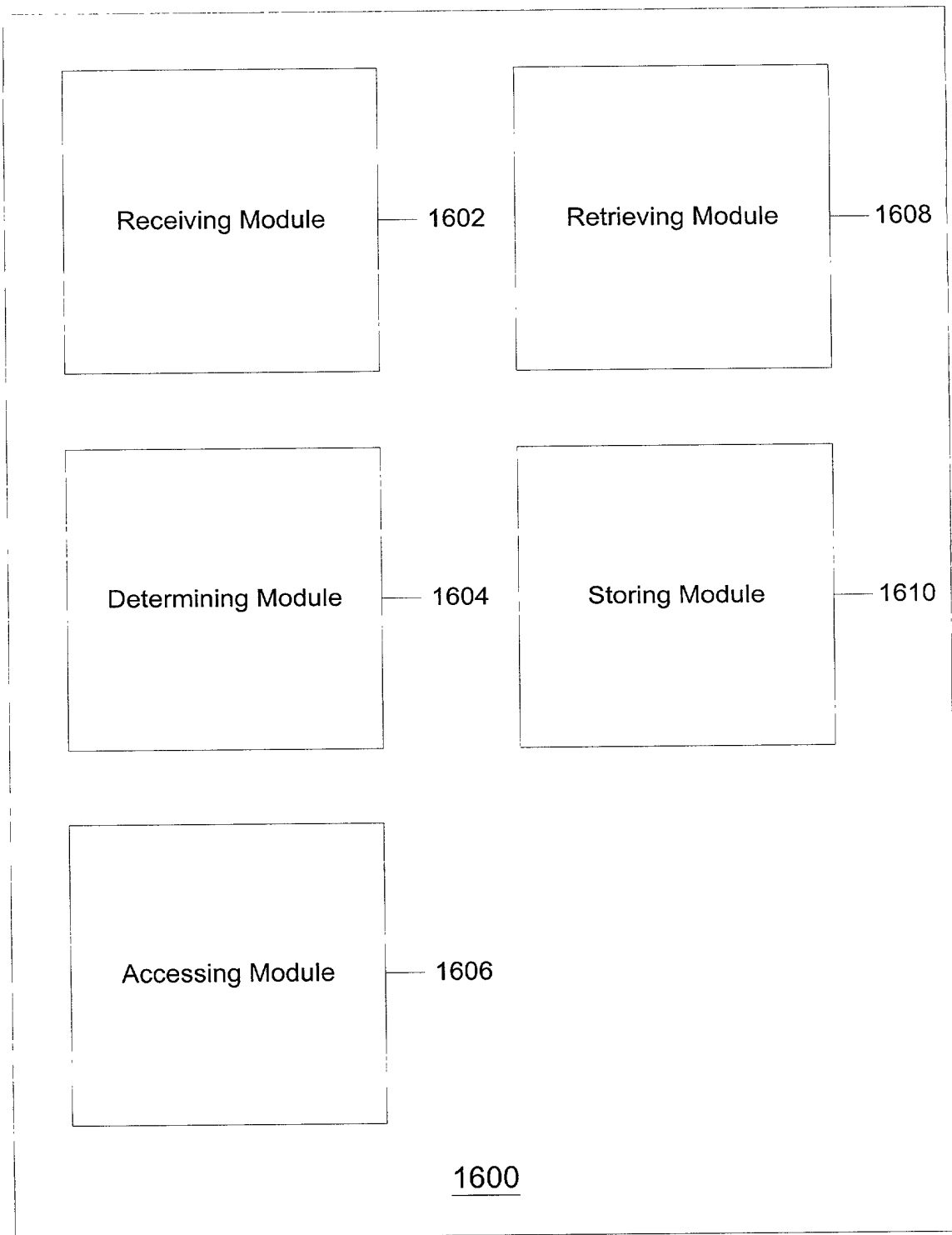


Figure 16